6N137

Super **High** Speed Response **OPIC Photocoupler**

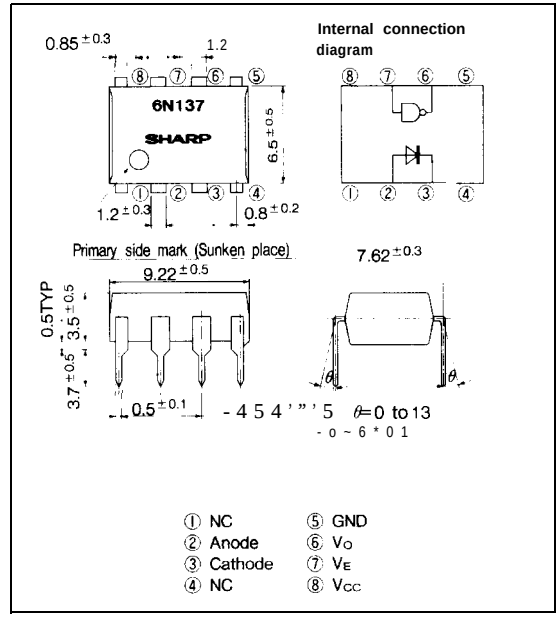
■ Features

1. Super high speed response
   (t_{PHL}, t_{PLH}: TYP. 45ns at $R_L = 350\Omega$)
2. Isolation voltage between input and output
   V_{iso} :2 500V_{rms}
3. Low input current drive (I_{FHL}: MAX. 5mA)
4. Instantaneous common mode rejection voltage
   CMH : TYP. 500V/ μS
5. LSTTL and TTL compatible output
6. Recognized by UL , file No. E64380

■ Applications

1. High speed interfaces for computer peripherals, microcomputer systems
2. High speed line receivers
3. Noise reduction
4. Interfaces for data transmission equipment

■ Outline Dimensions (Unit : mm)



"OPIC" (Optical IC) is a **trademark of the** SHARP **Corporation**
An OPIC consists of a light-detecting element and signal-processing circuit integrated onto a single chip.

■ **Absolute** Maximum Ratings (Ta = 25℃)

Parameter		Symbol	Rating	Unit
Input	*1 Forward current	I_F	20	mA
	*2 Peak forward current	I_F	40	mA
	Reverse voltage	V_R	5	V
output	Supply voltage	V_{CC}	7	V
	Enable voltage	C_E	5.5	v
	High level output voltage	V_{OH}	7	v
	Low level output current	I_{OL}	50	mA
	Output collector power dissipation	P_C	85	mW
*5 Isolation voltage		V_{iso}	2 500	V_{rms}
Operating temperature		T_{opr}	o to +70	℃
Storage temperature		T_{stg}	−55 to +125	℃
*6 Soldering temperature		T_{sol}	260	℃

*1 Ta=O to 70℃
*2 Pulse width ≦ lms
*3 For 1 minute MAX.
*4 Not exceed 500mV or more than supply voltage (V_{CC})
*5 AC for 1 minute, 4[) to 60% RH
Apply the specific voltage between all the input electrode pins connected together and all the output electrode pins connectecf together.
*6 2mm or more away from the lead base for 10 seconds

■ Electro-optical Characteristics (Ta = O to+ 70"C unless otherwise specified)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Logic (1) output current	Ion	V_{CC}=5.5V, V_O=5.5V, I_F=250 μA, V_E=2.0V	—	2	250	μA
Logic (0) output voltage	V_{OI}	V_{CC}=5.5V, I_F=5mA, V_{EH}=2.0V, I_{OL} (Sinking) =13mA	–	0.4	0.6	V
Logic (1) enable current	I_{EH}	V_{CC}=5.5V, V_E=2.0V		–0.8	–	mA
Logic (0) enable current	I_{EI}	V_{CC}=5.5V, V_E=0.5V	—	–1.2	–2.0	mA
Logic (1) supply current	I_{CCH}	V_{CC}=5.5V, I_F=0mA, V_E=0.5V	—	7	15	mA
Logic (0) supply current	I_{CCL}	V_{CC}=5.5V, I_F= 10mA, V_E=0.5V		13	18	mA
*1Leak current	I_{I-O}	45% RH Ta=25℃, t=5s, V_{I-O}=3 000V$_{dc}$			1.0	μA
*1Isolation resistance (input-output)	R_{I-O}	V_{I-O}=500V, Ta=25℃		10^{12}	—	Ω
*1Capacitance (input output)	C_{I-O}	f=1MHz, Ta=25℃	—	0.6		pF
*2Input forward voltage	V_F	I_F= 10mA, Ta=25℃	—	1.6	1.75	v
Input reverse volt age	BVR	I_R=10 μA, Ta=25℃	5	—		V
Input capacitance	C_{IN}	V_F=0, f=1 MHz		60	—	pF
*3Current transfer ratio	CTR	I_F=5.0mA, R_L = 100Ω	—	700	–	%
'propagation delay time output (o) → (1)	t_{PLH}	Ta=25℃ V_{CC}=5V, R_I=350Ω C_I= 15pF, I_F=7.5mA	–	45	75	ns
*5Propagation delay time output (1) → (o)	t_{PHL}	Ta=25℃, V_{CC}=5V, R_I=350Ω, C_I=15pF, I_F=7.5mA	–	45	75	ns
Output rise-fall time (10 to 90%)	t_r, t_f	R_L=350Ω, C_L =15pF, I_F=7.5mA		20, 30	–	ns
'Enable propagation delay time (1) • (0)	t_{ELH}	R_L=350Ω C_I=15pF, I_F= 7.5mA, V_{EH}=3.0V, V_{EI}=0.5V	–	40		ns
*7Enable propagation delay time (0) → (1)	t_{EHL}	R_I=350Ω, C_I=15pF, I_F=7.5mA, V_{EH}=3.0V, V_{EL}=0.5V	–	15		ns
'Instantaneous common mode rejection VOI tage "output (o)"	CM_H	V_{CM}=10V, R_I=350Ω, V_O (min.)=2V, I_F=0mA	—	500	—	V/μs
'Instantaneous common mode rejection voltage "output (1)"	CM_L	V_{CM}=10V, R_I=350Ω, V_O (min. I-0.8\;, I_F=5mA	–	—500	—	V/μs

Note) Typical values are all at V_{CC} 5V, Ta = 25℃

*1 Measured as 2-pin element, Connect pins 2 and 3, connect pins 5, 6, 7 and 8.

*2 At I_F=10mA, V_F decreases at the rate of 1.6mV/℃ if the temperature goes up.

*3 DC current transfer ratio is defined as the ratio of output collector current to forward bias input current.

*4, *5 Refer tn the Fig. 1.

*6, *7 Refer to the Fig. 2.

*8 CM_H represents a common mode voltage ignorable rise time ratio that can hold logic (1) state in output
CM_L represents a common mode voltage ignorable fall time ratio that can hold logic (0) state in Output

■ Recommended Operating Conditions

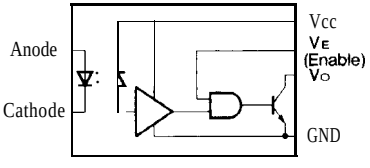
Parameter	Symbol	MIN.	MAX.	Unit
Low level input current	I_{FL}	0	250	μA
High level input current	I_{FH}	*6.3	15	mA
High level enable voltage	V_{EH}	2.0	V_{CC}	V
Low level enable voltage	V_{EL}	0	0.8	V
Supply voltage	V_{CC}	4.5	5.5	v
Fanout (TTL load)	N	—	8	—
Operating temperature	T_{opr}	0	70	℃

1 No necessary external pull-up resistor to hold enable input at high level

2. Connect a ceramic by-pass capacitor (0.01 to 0.1 μF) between V_{CC} and GND at the position within I cm from pin.

3. *20% giard band, switching threshold for degradation of CTR are 5mA or less at initial value.

Circuit Block Diagram

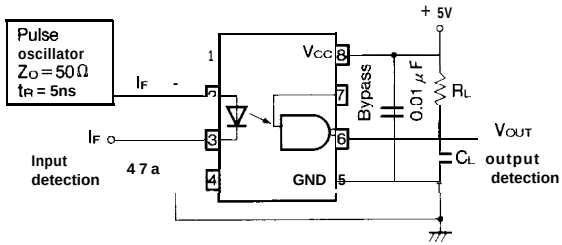


Truth Table

Input	Enable	Output
H	H	L
L	H	H
H	L	H
L	L	H

L: Logic (0) H: Logic (1)

Fig.1 Test Circuit for Propagation Delay time



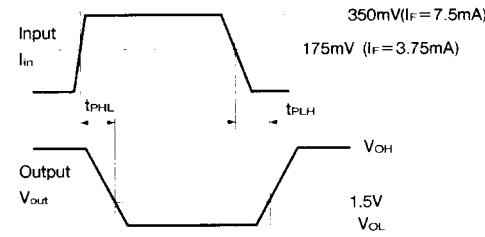
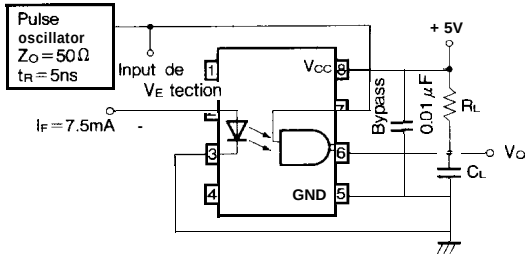


Fig.2 Taat **Circuit** for **Enable Propagation Delay Time**



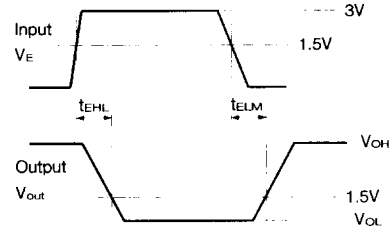
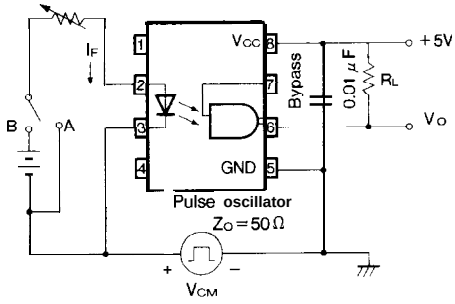


Fig.3 Taat Circuit for **Instantaneous** common Mods **Rejection Voltage**



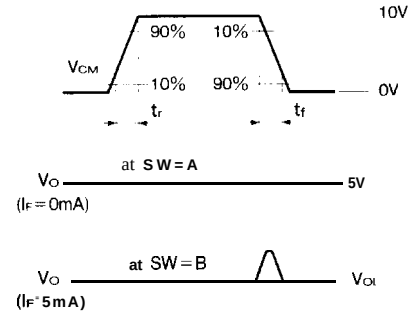


Fig. 4 Output Collector Power Dissipation vs. Ambient Temperature

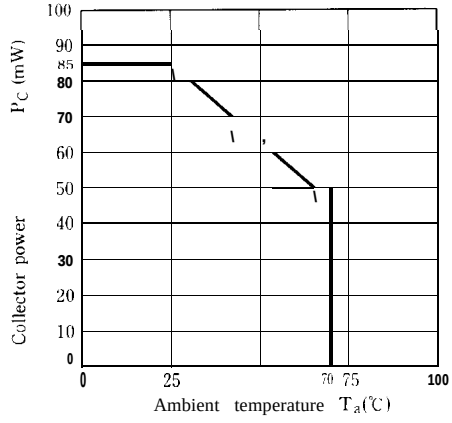


Fig. 5 Forward **Current vs. Forward Voltage**

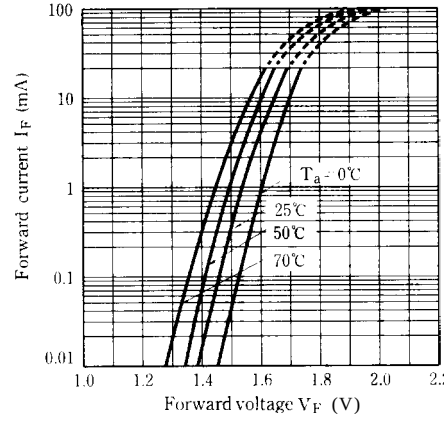


Fig. 6 High Level Output Current vs. Ambient Temperature

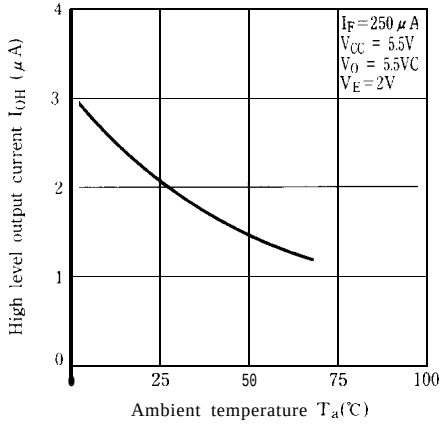


Fig. 7 Low Level Output Voltage vs. Ambient Temperature

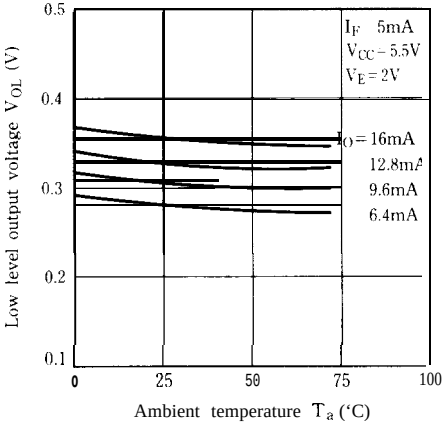


Fig. 8-a Output Voltage vs. Forward Current

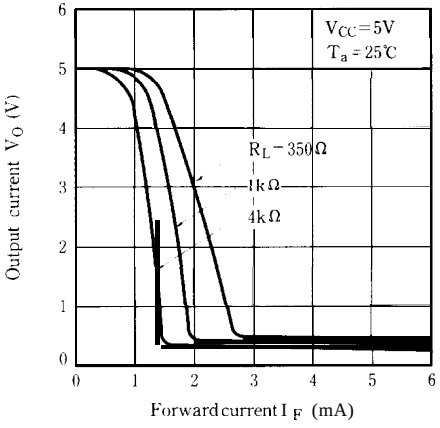


Fig. **8-b Output Voltage vs.** Forward Currant **(Ambient Temp. Characteristics)**

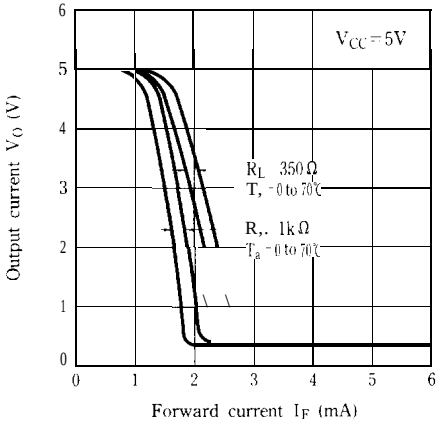


Fig. 9 Propagation Delay Time vs. Forward Current

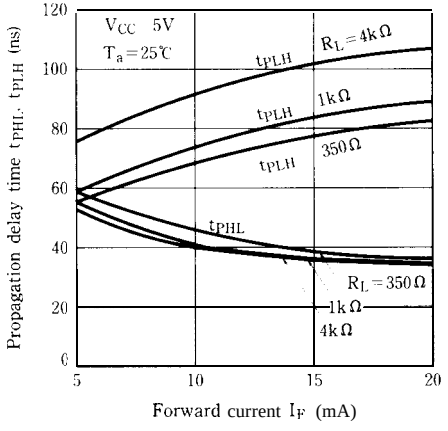


Fig.10 Propagation Delay Time vs. Ambient Temperature

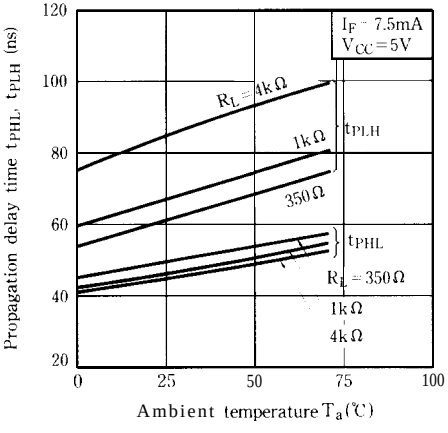


Fig.11 Rise Time, Fall Time vs. Ambient Temperature

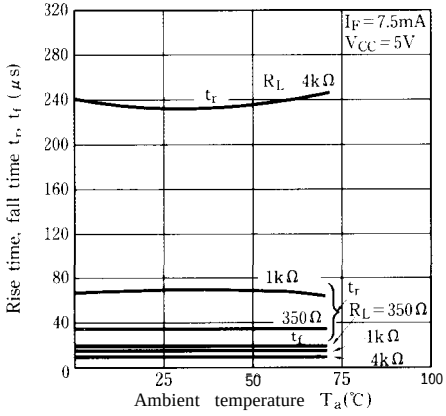
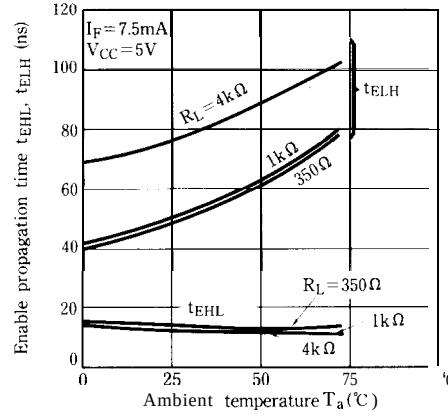


Fig.12 Enable Propagation Time vs. Ambient Temperature



■ mecautionsf oruse

- Handle this product the same as with other integrated circuits against static electricity.
- Please refer to the chapter “Precautions for Use” . (Page 78 to 93)